FPGA Altera

(ep4ce22f17c6)

(0)29 VCC3P3

(0)19

(0)20

(0)21

(0)22

(0)30 GND

(1)11

(1)12

(1)13

(1)14

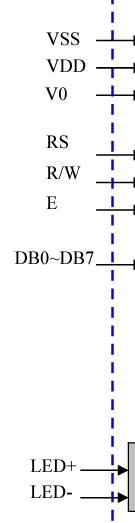
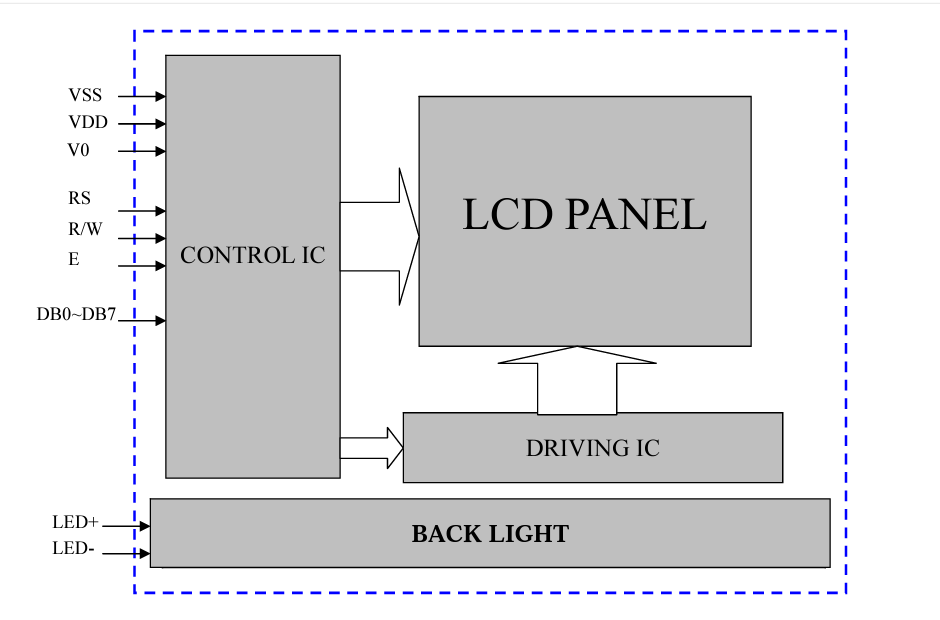
(1)15

(1)16

(1)17

Diagram, schematic

Description automatically generated



LM35

0



clk

10 bits

rst

Counter 9 to 0

Register

en

rst

10 bits

clk

00100101

B

Comparator greater

A

S

Red LED

Green LED

DEMUX 2x1

Active LED